

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes a column decoder and a first row decoder. The column decoder or first row decoder includes a level shift circuit having  
5 a second to fifth transistor and a first switch element. The second and third MOS transistors have source connected electrically to a power supply potential. The fourth MOS transistor has a gate receiving an input signal, drain connected to a drain  
10 of the second MOS transistor and to the gate of the third MOS transistor, and the source connected to the ground potential. The fifth MOS transistor has a gate receiving the inverted input signal, drain connected to a drain of the third MOS transistor, to the gate of the  
15 second MOS transistor and to a bit line or word line. The first switch element controls the supply of the power supply potential to the second and third MOS transistors.